

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4070B

### gates

### Quadruple exclusive-OR gate

Product specification  
File under Integrated Circuits, IC04

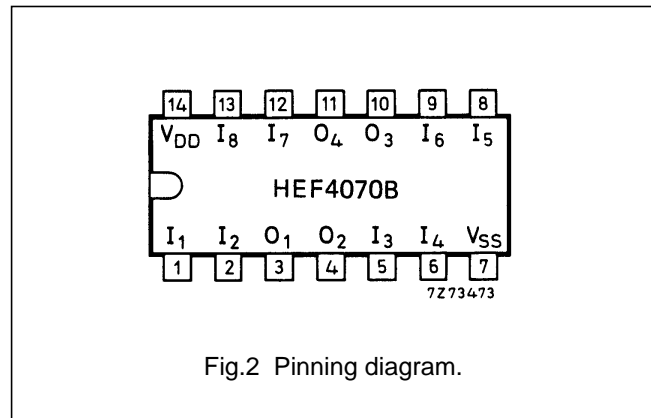
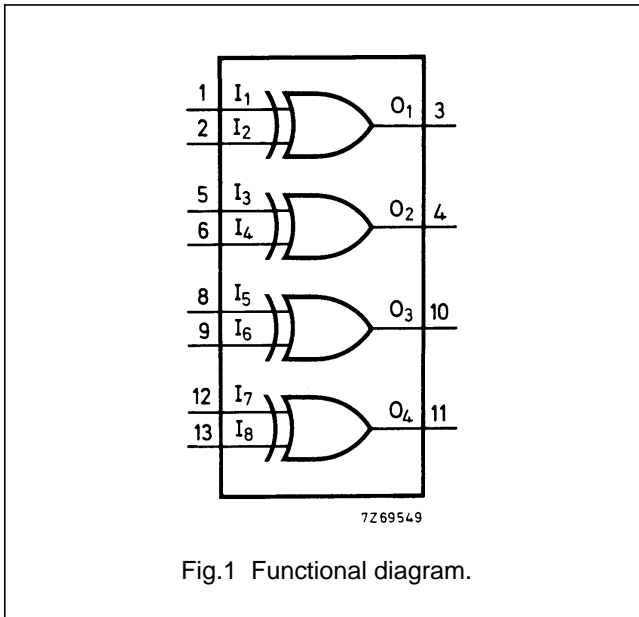
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# Quadruple exclusive-OR gate

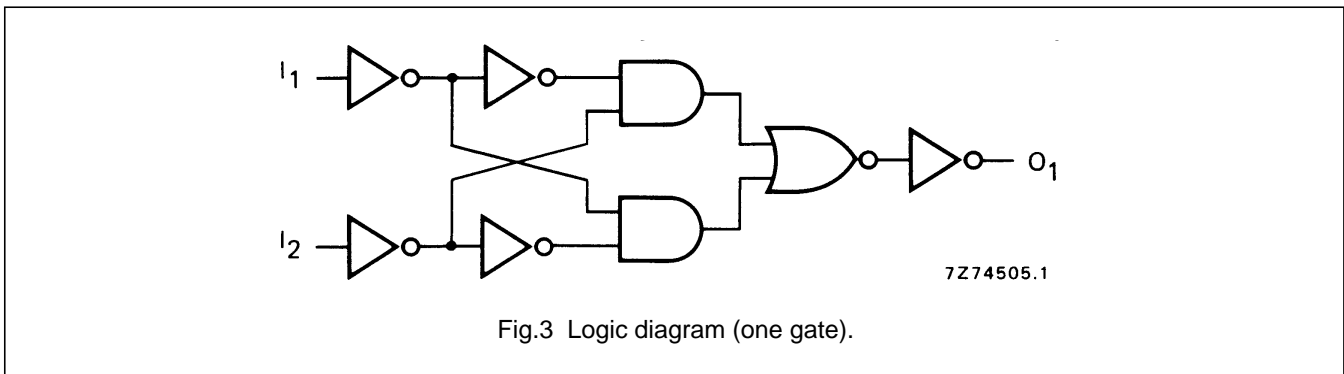
# HEF4070B gates

### DESCRIPTION

The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4070BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4070BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4070BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America



### APPLICATION INFORMATION

Some examples of applications for the HEF4070B are:

- Logical comparators
- Parity checkers and generators

### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications

### TRUTH TABLE

I <sub>1</sub>	I <sub>2</sub>	O <sub>1</sub>
L	L	L
H	L	H
L	H	H
H	H	L

### Note

1. H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)

# Quadruple exclusive-OR gate

# HEF4070B gates

## AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	85	175	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		35	75	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	55	ns	$21\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	75	150	ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		30	65	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$1100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$4900 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$14\,400 f_i + \sum (f_o C_L) \times V_{DD}^2$	